CLAIMS

1. A method of forming a differential transistor comprising:

forming an enhancement mode transistor of a first conductivity type having a source coupled to a source of a depletion mode transistor of a second conductivity type; and

forming a threshold voltage of the enhancement mode transistor so that an absolute value of the threshold voltage of the enhancement mode transistor is no greater than an absolute value of a threshold voltage of the depletion mode transistor.

2. The method of claim 1 further including coupling a gate of the enhancement mode transistor to be driven by a first signal and coupling a gate of the depletion mode transistor to be driven by a second signal.

3. The method of claim 2 wherein coupling the gate of the enhancement mode transistor to be driven by the first signal and coupling the gate of the depletion mode transistor to be driven by the second signal includes coupling the gate of the enhancement mode transistor and the gate of the depletion mode transistor to be driven by out of phase signals.

4. The method of claim 1 further including forming a drain of the enhancement mode transistor to be coupled to a first signal and forming a drain of the depletion mode transistor to be coupled to a second signal.

5. The method of claim 4 further including coupling the drain of the enhancement mode transistor to a first signal, coupling a gate of the enhancement mode transistor to a gate of another enhancement mode transistor, coupling the drain of the depletion mode transistor to a voltage return, coupling a gate of the depletion mode transistor to a gate and a drain of another depletion mode transistor and to a drain of the another enhancement mode transistor, coupling a source of the another enhancement mode transistor to receive a voltage from a voltage source.

6. The method of claim 5 wherein coupling the drain of the enhancement mode transistor to the first signal includes coupling the drain of the enhancement mode transistor to a first terminal of a resistor and to a signal input of a microprocessor, and coupling a second terminal of the resistor to receive the voltage from the voltage source.

7. The method of claim 5 further including coupling a source of the another depletion mode transistor to the voltage return.

8. The method of claim 5 further including coupling a source of the another depletion mode transistor to a drain of a lower output transistor and coupling a source of the lower output transistor to the voltage return.

9. The method of claim 4 further including coupling the drain of the depletion mode transistor to receive a first signal, coupling a gate of the depletion mode transistor to a gate of another enhancement mode transistor, coupling the drain of the enhancement mode transistor to a voltage return, coupling a gate of the enhancement mode transistor to a drain of another depletion mode transistor and to a drain of the another enhancement mode transistor, coupling a source of the another depletion mode transistor to a gate of the another depletion mode transistor, and coupling a source of the another enhancement mode transistor to receive a voltage from a voltage source.

10. The method of claim 9 wherein coupling the drain of the depletion mode transistor to receive the first signal includes coupling the drain of the depletion mode transistor to a first terminal of a resistor and to a signal input of a microprocessor and coupling a second terminal of the resistor to receive the voltage from the voltage source.

11. The method of claim 9 further including coupling the source of the another depletion mode transistor to the voltage return.

12. The method of claim 9 further including coupling a source of the another depletion mode transistor to a drain of a lower output transistor and coupling a source of the lower output transistor to the voltage return.

13. A differential transistor comprising:

a depletion mode MOS transistor of a first conductivity type having a first source, a first drain, a first gate, and a first threshold voltage; and

an enhancement mode MOS transistor of a second conductivity type having a second source connected to the first source, a second drain, a second gate, and a second threshold voltage having an absolute value that is less than an absolute value of the first threshold voltage.

14. The differential transistor of claim 13 wherein the first gate is coupled to receive a first signal and the second gate is coupled to receive a second signal.

15. The differential transistor of claim 14 wherein the first gate is coupled to receive the first signal and the second gate is coupled to receive the second signal that is out of phase with the first signal.

16. The differential transistor of claim 13 further including the first drain coupled to a first terminal of a resistor and to a signal input of a microprocessor and a second terminal of the resistor coupled to a voltage source.

17. The differential transistor of claim 16 further including the second drain coupled to a voltage return.

18. The differential transistor of claim 13 further including the second drain coupled to a first terminal of a resistor and to a signal input of a microprocessor, a second terminal of the resistor coupled to a voltage source, the first drain coupled to a voltage return.

19. A method of operating a differential transistor comprising:

providing an enhancement mode transistor of a first conductivity type having a source, a gate, and a drain coupled to a receive a first signal;

providing a depletion mode transistor of a second conductivity type having a source coupled to the source of the enhancement mode transistor, a gate, and a drain coupled to a receive a second signal;

applying a differential voltage between the gate of the enhancement mode transistor and the gate of the depletion mode transistor that is greater than a first voltage to enable conduction between the drain of the enhancement mode transistor and the drain of the depletion mode transistor; and

applying a differential voltage between the gate of the enhancement mode transistor and the gate of the depletion mode transistor that is less than the first voltage to disable conduction between the drain of the enhancement mode transistor and the drain of the depletion mode transistor.

20. The method of claim 19 wherein providing the enhancement mode transistor and providing the depletion mode transistor includes providing the enhancement mode transistor having an absolute value of a threshold voltage of the enhancement mode transistor to be no greater than an absolute value of a threshold voltage of the depletion mode transistor, and wherein applying the differential voltage between the gate of the enhancement mode transistor and the gate of the depletion mode transistor that is greater than the first voltage includes applying the differential voltage having a value that is greater than zero volts.